

October 1987
Revised January 1999

CD4069UBC
Inverter Circuits

General Description

The CD4069UB consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C907, and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} typ.
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MM74C04

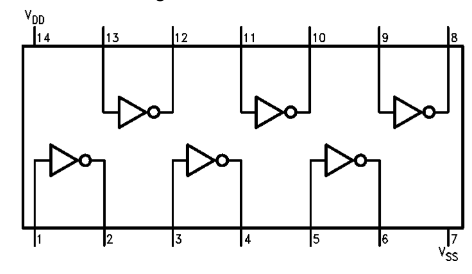
Ordering Code:

Order Number	Package Number	Package Description
CD4069UBCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
CD4069UBCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4069UBCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

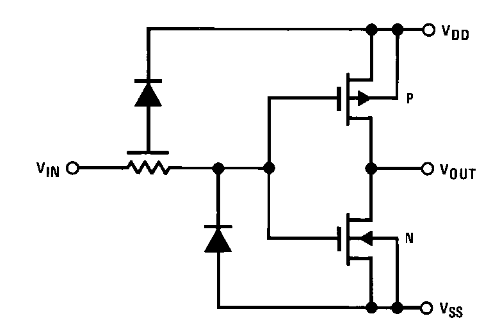
Device also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

Connection Diagram

Pin Assignments for SOIC and DIP



Schematic Diagram



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Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5V to +18 V_{DC}
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and Electrical Characteristics table provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
V_{OL}	LOW Level Output Voltage	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	LOW Level Input Voltage	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V		1.0			1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0			2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0			3.0		3.0	V
V_{IH}	HIGH Level Input Voltage	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0			4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0			8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0			12.0		V
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

Note 3: V_{SS} = 0V unless otherwise specified.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5)

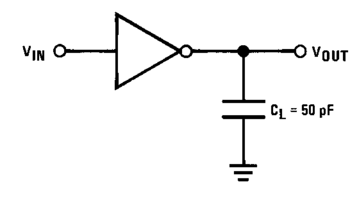
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, t_r and $t_f \leq 20$ ns, unless otherwise specified

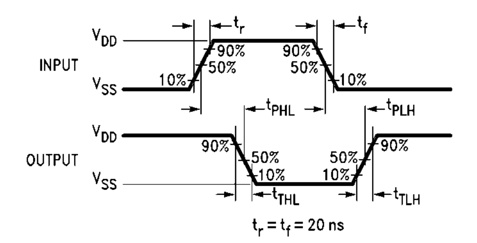
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	$V_{DD} = 5V$		50	90	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		80	150	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Gate		6	15	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 6)		12		pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note—AN-90.

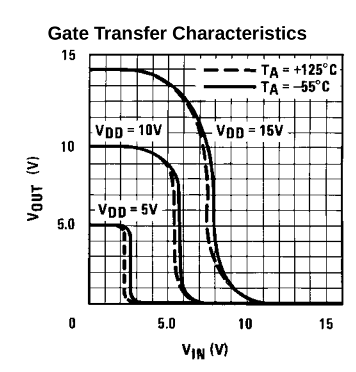
AC Test Circuits and Switching Time Waveforms



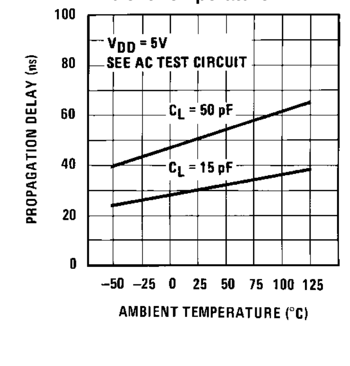


Typical Performance Characteristics

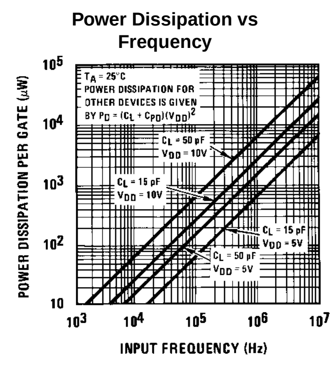
Gate Transfer Characteristics



Ambient Temperature

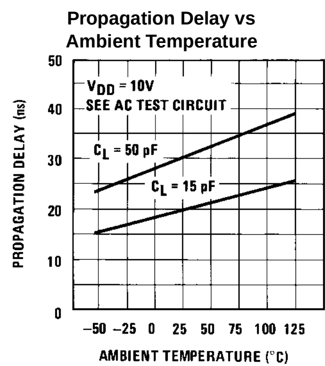


Power Dissipation vs Frequency

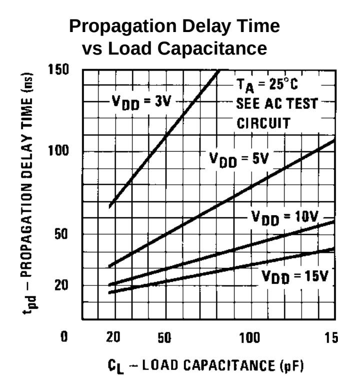


Propagation Delay vs

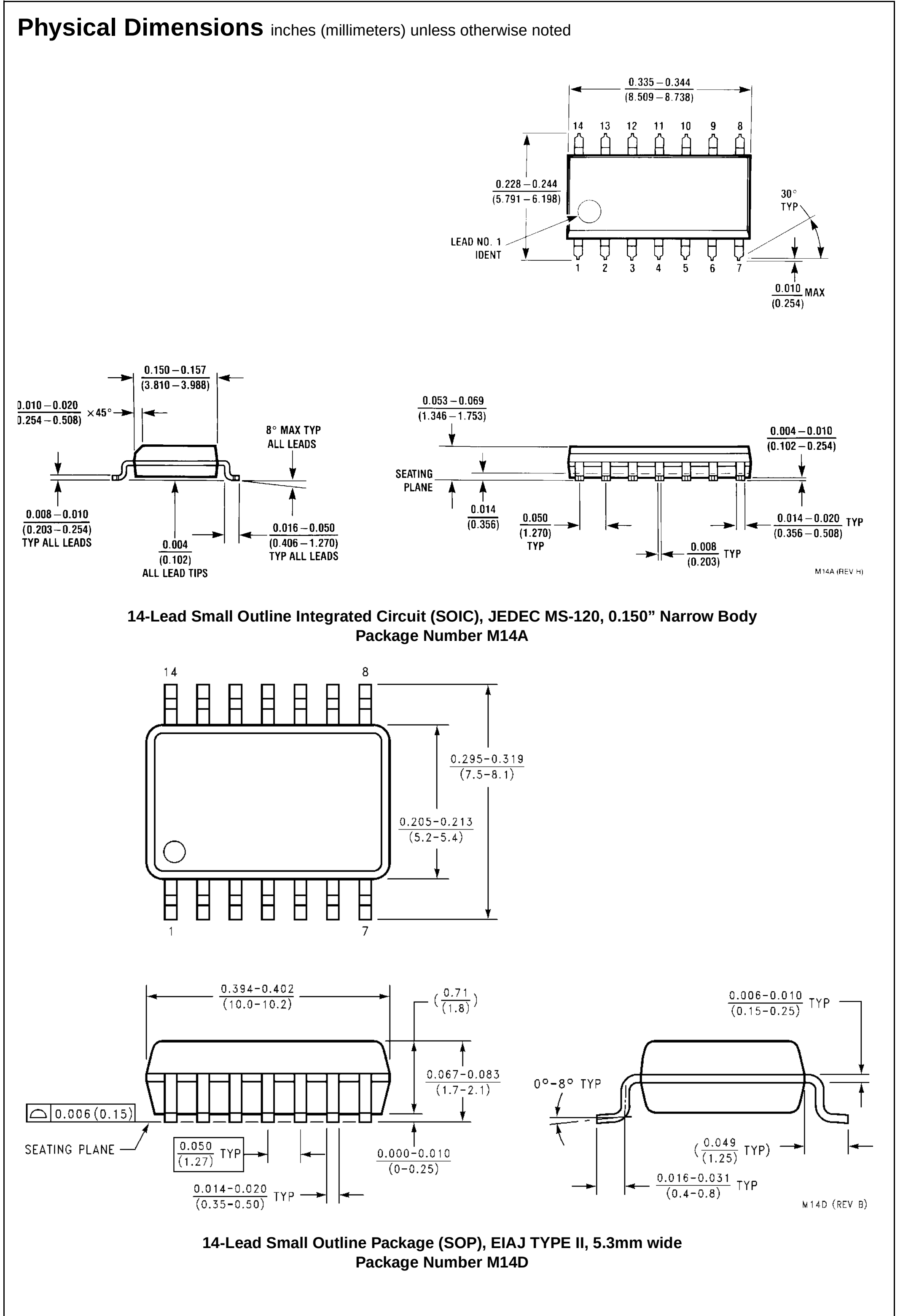
Propagation Delay vs Ambient Temperature



Propagation Delay Time vs Load Capacitance



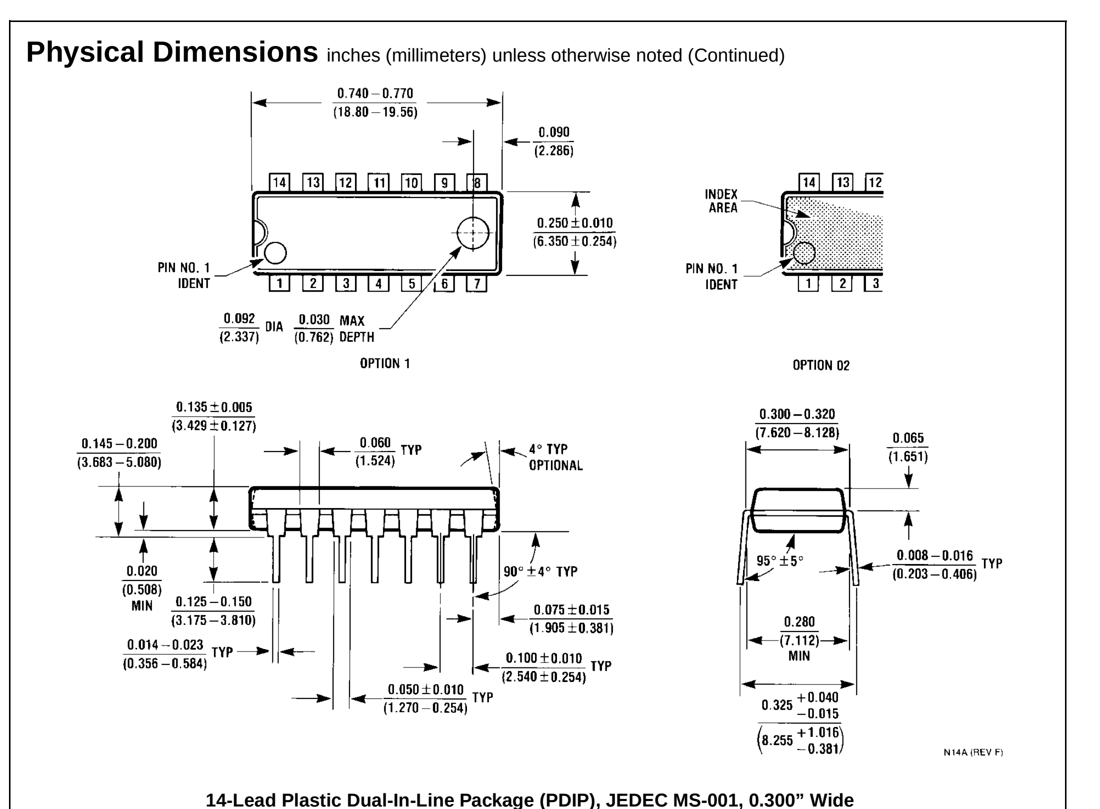
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow Body
Package Number M14A

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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